WHAT IS CLAIMED IS:

1. A system for measuring fault coverage in an integrated circuit (IC), comprising:

a Device Under Test (DUT) assembly including said IC, wherein said IC includes at least one node operable to be stimulated to a stuck-at fault condition by a certain frequency of electromagnetic (EM) radiation;

a probe operable to stimulate said DUT assembly with said frequency of EM radiation; and

a test pattern generator and interface system interfacing with said DUT assembly, said test pattern generator and interface system operating to apply a test vector to said DUT assembly and receive a corresponding response, wherein said corresponding response is indicative of a fault coverage measurement.

2. The system for measuring fault coverage in an IC as recited in claim 1, wherein said IC is disposed on a die.

3. The system for measuring fault coverage in an IC as recited in claim 1, wherein said IC is disposed on a wafer.

4. The system for measuring fault coverage in an IC as recited in claim 1, wherein said IC is disposed on a packaged chip.

5. The system for measuring fault coverage in an IC as recited in claim 1, wherein said probe comprises a laser voltage probe.

6. The system for measuring fault coverage in an IC as recited in claim 1, wherein said stuck-at fault condition comprises a stuck-at-zero condition.

7. The system for measuring fault coverage in an IC as recited in claim 1, wherein said stuck-at fault condition comprises a stuck-at-one condition.

8. A method for measuring fault coverage in an integrated circuit (IC), comprising:

stimulating a select number of nodes associated with said IC with a certain frequency of electromagnetic (EM) radiation;

creating a stuck-at fault condition at said select number of nodes;

applying a test vector set to said IC upon creating said stuck-at fault condition;

comparing said IC's output against expected results associated with said test vector set; and

determining fault coverage as a percentage of said stuck-at fault conditions detected by said test vector set.

9. The method as recited in claim 8, wherein said certain frequency of EM is supplied by a laser voltage probe system.

10. The method as recited in claim 8, wherein said stuck-at fault condition comprises a stuck-at-zero condition.

11. The method as recited in claim 8, wherein said stuck-at fault condition comprises a stuck-at-one condition.

12. A system for measuring fault coverage in an integrated circuit (IC), comprising:

means for stimulating a stuck-at fault condition in a select number of nodes associated with said IC with a certain frequency of electromagnetic (EM) radiation;

means for applying a test vector set to said IC upon creating said stuck-at fault condition;

means for comparing said IC's output against expected results associated with said test vector set; and

means for determining fault coverage as a percentage of said stuck-at fault conditions detected by said test vector set.

13. The system for measuring fault coverage in an IC as recited in claim 12, wherein said means for stimulating a stuck-at fault condition comprises a laser voltage probe system.

14. The system for measuring fault coverage in an IC as recited in claim 12, wherein said stuck-at fault condition comprises a stuck-at-zero condition.

15. The system for measuring fault coverage in an IC as recited in claim 12, wherein said stuck-at fault condition comprises a stuck-at-one condition.